

CRACK STOP FOR LOW K DIELECTRICS

Abstract

A crack stop for low K dielectric materials of an integrated circuit (IC) formed on an IC chip using metal interconnects which do not form a self-passivating oxide layer, such as copper or silver interconnects, in a low-K dielectric material to prevent damage to the active area of the IC chip caused by chipping and cracking formed along peripheral edges of the IC chip during a dicing operation. A moisture barrier or edge seal is formed as a metal stack positioned along the outer peripheral edges of the active area of the IC chip. The crack stop is formed by at least one trench or groove positioned outside of the moisture barrier/edge seal on the outer periphery of the IC chip.